SEA INC OF DELAWARE

PRELIMINARY MAINTENANCE MANUAL

EXCERPTS ON THEORY OF OPERATION

MF/HF SSB GMDSS RADIOTELEPHONE/DSC CONTROLLER

MODEL SEA 245

SEA, Inc.

7030 220th St. S.W.

Mountlake Terrace, Washington 98043

(425) 771-2182

FAX: (425) 771-2650

TABLE OF CONTENTS

LIST OF FIGURES

5 THEORY OF OPERATION

5.1 GENERAL

The SEA 245 is a double conversion MF/HF SSB transceiver of up conversion design. The first intermediate frequency (IF) is 45 MHz and uses a relatively narrowband (8 kHz) crystal topping filter in conjunction with front end low and high pass filters to provide excellent image, spurious and harmonic rejection. This type of broadband design results in a minimum of tuned circuits. The second intermediate frequency of approximately 40 kHz permits the use of DSP oversampling techniques to provide secondary selectivity.

Receiver baseband recovery uses IF based DSP circuitry. The filtered, downconverted 40 kHz IF signal is fed into the ADC and DSP circuitry provides programmable receiver filtering and demodulation.

Transmitter baseband generation is likewise DSP based and uses the DSP/CODEC circuitry and an I/Q modulator, together with an appropriate DSP algorithm to generate the desired baseband signal at 45 MHz.

The frequency control circuitry in the SEA 245 uses a combination of two PLL-based frequency synthesizers and the system DSP engine to provide the various frequency conversions.

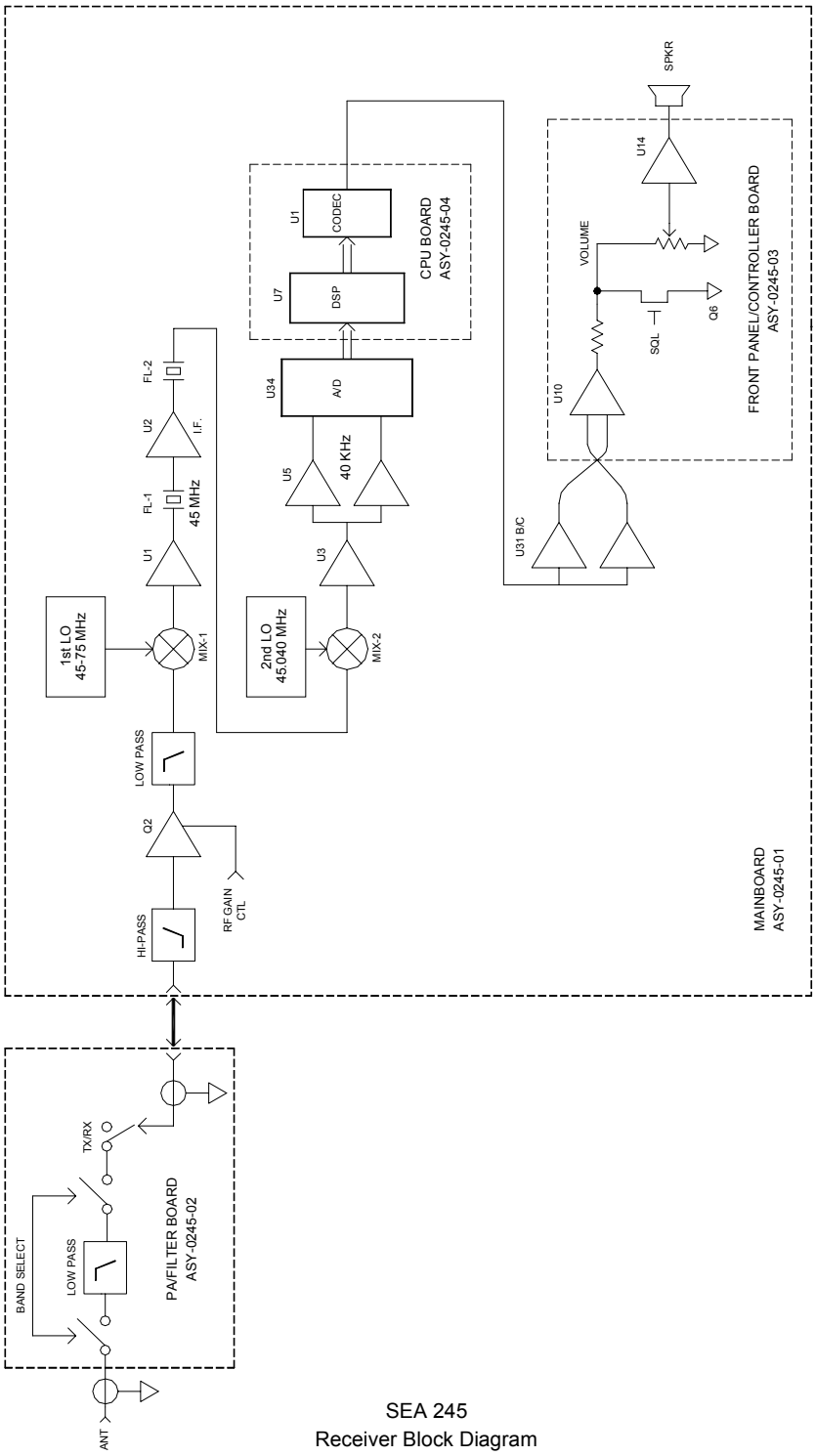
The first conversion oscillator is the 90-150 MHz VCO, which uses a PLL-based loop with a reference of 8 kHz. This oscillator is then divided by two to 45-75 MHz. The resulting coarse-tuned local oscillator has a resolution of 4 kHz, very fast settling time and a low noise floor.

The second conversion VCO operates at 45.040 MHz. In the transmit mode, the VCO operates at 45.016 MHz for the transmitter I/Q modulator circuitry. The loop reference frequency is 8 kHz.

All frequency determining circuitry is locked to the master clock oscillator, a 12.288 MHz OCXO.

The SEA 245 operating system resides in the Front Panel/Controller Assembly. The operator communicates with the operating system firmware through the 18 key keypad. The Front Panel/Controller Assembly is actually a SEAbuss(c) Controller designed to communicate with the Mainboard Controller through the standard SEABUSS interface. The SEA 245 SEABUSS is designed to support a single SEA 2450 Remote Controller in addition to the Front Panel.

5.2 THE RECEIVER



SEA 245
Receiver Block Diagram
Figure 5.2.1

5.2.1 BLOCK DIAGRAM

Figure 5.2.1 shows the block diagram of the receive mode. The received RF signal is routed from the rear panel antenna jack to a low pass filter selected by a relay bank on the PA/Filter Assembly (ASY-0245-02). The output of the filter is routed from J4 on the PA/Filter Assembly through a coaxial cable to the receiver input circuitry on the Mainboard Assembly (ASY-0245-01). The signal is further bandpass filtered to reject interfering signals and input to the RF preamplifier/attenuator, Q2. In the "on" state, the amplifier provides some 3-4 dB of low-noise preamplifier gain. In the "off" state, the stage becomes an attenuator that provides approximately 10 dB of signal attenuation. The use of this switched gain stage improves the weak signal sensitivity of the receiver and provides a front-end attenuator that is used to insure that large signals do not swamp the ADC in the DSP engine. The preamplifier/attenuator stage output is routed to the first mixer and the signal is upconverted to the first IF at 45 MHz.

The 45 MHz IF signal passes through a low noise MMIC gain stage to a 4-pole crystal "topping" filter with approximately 8 kHz bandwidth, a second MMIC amplifier stage and a second two-pole crystal filter into the second mixer. In the second mixer the signal is combined with the second Local Oscillator frequency of 45040 kHz. The mixer output signal is buffered by low-noise amplifier U3, converted to a push-pull signal by U5 and then applied to the input of the A/D converter U34. U34 digitizes the signal and passes it to the DSP engine, which provides all baseband filtering, fine-tuning, demodulation and AGC functions. The audio signal is converted to balanced format for transmission over the SEABUSS audio lines to the Front Panel/Controller board (ASY-0245-03). The Controller provides squelch processing, volume control and a speaker amplifier.

5.2.2 RECEIVE RF CIRCUITRY AND FIRST MIXER

As previously discussed, an incoming signal is first passed through some shared circuitry on the PA/Filter Board (ASY-0245-02). This consists of a bandswitched array of low pass filters, a T/R relay and a PIN diode signal limiter which prevents damage to receiver input circuitry in the presence of extremely large signals. The received signal is then sent through a coaxial cable to the receiver input on the Mainboard Assembly (ASY-0245-01). On the Mainboard, a high-pass filter consisting of C1, L1 and C7 further filters the signal.

Diode CR1 is forward biased in the receive mode from the +12VRX rail and reversed biased in the transmit mode from the +12VTX rail through CR2. This T/R switching circuitry provides extra isolation between the low-level transmitter signal and any signal leakage through the PA/Filter Board T/R switches. From CR1, the received signal passes through a low-pass filter (C5, L2 and C6) to the preamplifier/attenuator stage. This stage is a low noise, low gain (+4 dB) broadband common-gate JFET amplifier. A gain step is provided by switching the preamplifier supply voltage on and off through Q6. When Q6 is OFF, the stage

becomes an attenuator with a loss of approximately 10 dB. The output of the preamplifier is then applied to double-balanced mixer MIX1. The use of a hot carrier diode mixer assures minimal cross modulation and intermodulation distortion in the receiver front end.

5.2.3 THE 45 MHz IF

The output from mixer MIX1 contains the desired signal upconverted to 45 MHz. This signal is amplified by a low noise, high dynamic range MMIC amplifier that establishes a good low noise 50-ohm termination for the mixer. Output of the first IF amplifier is filtered by FIL1, a four-pole monolithic crystal filter of approximately 8 kHz bandwidth. This is the "topping" filter, which serves to remove the unwanted secondary image, RF, and LO leakage as well as other unwanted upconverted HF signals that fall outside the filter bandwidth. Following the topping filter is a second MMIC amplifier stage and a second 2-pole filter. The total gain between the receiver input and the 45 MHz output is approximately 12 dB. The maximum allowable input signal with preamplifier on is approximately -3 dBm. Switching in the attenuator raises this level to approximately +10 dBm.

5.2.4 THE SECOND MIXER/POST AMPLIFIER

The second mixer converts the 45 MHz IF signal down to the second IF frequency of approximately 40 kHz. This mixer is a +13 dBm type, necessary to handle the somewhat higher signal levels present at this point. Following the mixer, the signal is passed through a low noise operational amplifier with a stage gain of 10 to a phase splitter circuit with stage gain of unity. The phase splitter output drives the differentially configured A/D input.

5.2.5 THE A/D CONVERTER

In IF/DSP receivers, system performance is highly dependent upon the characteristics of the A/D converter that moves the signal from the analog to the digital realm. In the SEA 245, A/D Converter U34 is a 24-bit, 96 kHz stereo ADC with a dynamic range of 110 dB and greater than 100 dB signal-to-noise ratio. The inputs to the ADC are full differential and the chip includes a reference filter and a digital decimation filter, which minimizes requirements for anti-aliasing filtering.

The 40 kHz second IF signal from the main receiver and the 14.583 kHz second IF signal from the 2187.5 kHz monitor receiver are each connected to one of the stereo inputs of the ADC. The resulting digitized signals are then passed on to the system DSP that is located on the CPU Board (ASY-0245-04).

5.2.6 THE CODEC

The CODEC is part of the CPU Board Assembly (ASY-0245-04) and uses AC'97 REV 1.03 architecture in a 18-bit sigma/delta configuration. The CODEC contains both an A/D and a D/A converter. The A/D converter is used to convert transmitter baseband signals into a digital bit stream suitable for processing in the DSP.

The D/A converter works in both receive and transmit modes. While receiving, digitally processed receiver signals from the DSP engine are converted back into the analog realm for processing through the amplifier/loudspeaker system. When transmitting, digitally processed (and generated) baseband signals from the DSP engine become the analog input signals to I/Q modulator chip U6 on the Mainboard Assembly.

5.2.7 THE DIGITAL SIGNAL PROCESSOR

The main DSP engine in the SEA 245 consists of U7 on the CPU Board Assembly. This is a TMS320VC5402, a specialized type of microprocessor which includes such features as a 40-bit ALU, data bus with Bus-Holder feature, extended addressing mode for 1Mx16-bit maximum external program space and many other specialized features intended to facilitate the specialized math functions necessary for DSP.

In the SEA 245, the DSP circuitry and firmware perform most of the signal processing functions necessary to convert a radio signal into an audio signal and vice-versa. These functions include frequency conversion, filtering, demodulation and gain control in the receive mode and baseband signal processing, filtering and generation in the transmit mode.

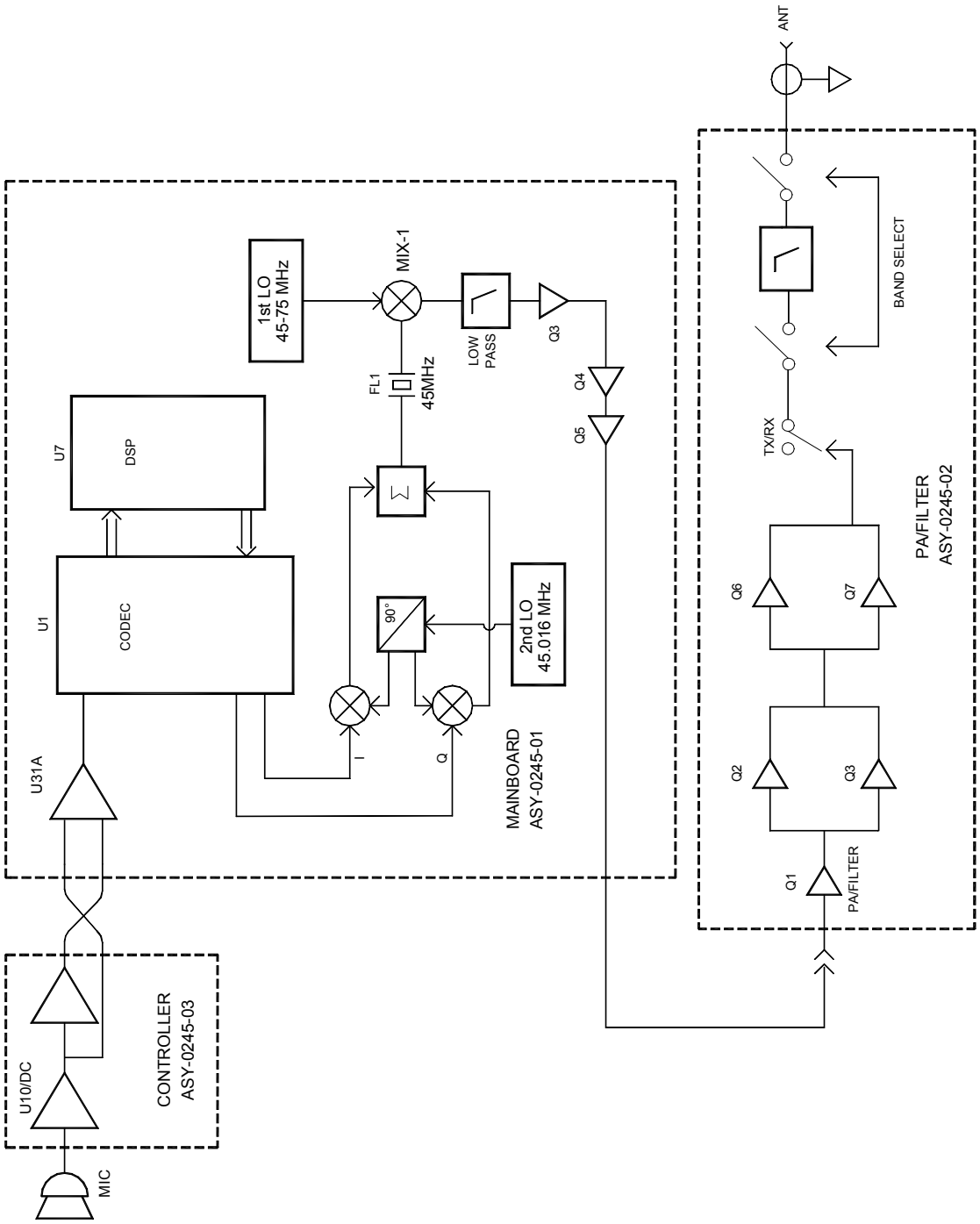
Since the DSP engine is actually a highly specialized type of microprocessor many, indeed most, of the characteristics of the receiver and transmitter functions are controlled by firmware algorithms embedded in the CPU Board memory. It is thus possible to use the same system digital hardware to generate (and demodulate) voice signals, TELEX signals, Digital Selective Calling signals or essentially any signal format up to the bandwidth limitations of the system analog hardware. Receiver AGC characteristics, transmitter bandwidth shaping and ALC functions are all determined in firmware.

5.2.8 THE RECEIVER AGC SYSTEM

There is only one variable gain element in the receiver AGC system, JFET preamplifier Q2. The amplifier passes signals whether or not it is enabled but, when disabled, there is approximately 10 dB of attenuation with respect to the enabled state. The actual AGC parameters are determined by the DSP algorithm and are tailored to suit the mode selected. When receiving SSB signals, the AGC has the usual fast attack-slow release characteristics suitable for SSB. The DSP software monitors signal level and disables the preamplifier when necessary to protect the A/D input from overload.

5.2.9 THE RECEIVER AUDIO CIRCUITY

The received signal is processed through the DSP engine and converted to an audio baseband signal in the system CODEC. This signal then exits the CPU Board as the SPKR.AF signal on pin 19 of J3 on the Mainboard and then passes through audio gate U30C to the audio SEABUSS driver stage consisting of U31B and U31C.



SEA 245
Transmitter Block Diagram
Figure 5.3.1

The audio signal then leaves the Mainboard Assembly (ASY-0245-01) as a 600 ohm balanced 0 dBm level and is received by the SEABUSS audio receiver in the Front Panel/Controller Assembly consisting of balanced line amplifier U10A.

After passing through U10A, the signal is then sent to the VOLUME control and the squelch limiter U8A and U8B. The signal from the VOLUME control wiper then goes to AF Power Amplifier U14 where it is amplified to a 4-Watt level and is then sent to the loudspeaker.

The limited audio signal from U8A is sent to an input of the Controller microprocessor (U1) where it is used to generate the SQL signal. An algorithm in U1 senses the presence (or absence) of a voice signal in the limited audio signal and, when the Squelch function is activated, generates a SQL OUT signal. The SQL OUT signal is used to turn on the squelch gate transistor Q6 to silence the loudspeaker.

5.3 THE TRANSMITTER

5.3.1 BLOCK DIAGRAM

Figure 5.3.1 shows the block diagram of the SEA 245 in the transmit mode. Microphone audio is amplified and converted to a balanced format for transmission from the Front Panel/Controller Assembly to the Mainboard Assembly (ASY-0245-01) via the SEAbuss audio lines. On the -01 board it is converted back to unbalanced format and then digitally sampled by CODEC U1 on the CPU board (ASY-0245-04). The CODEC transfers the data serially to the DSP, U7. The DSP generates a SSB signal at the (nominal) subcarrier frequency of 16 kHz. The CODEC converts the digital sample stream back to analog format. The resulting I and Q SSB signals are fed back to the Mainboard and into the inputs of quadrature modulator U6. The modulator mixes the I and Q signals with in-phase and quadrature 45.016 MHz local oscillator signals. This results in a single sideband signal at the 45 MHz intermediate frequency. This IF signal is passed through the bilateral 45 MHz crystal filter into the IF port of mixer MIX1. This mixer downconverts the IF signal into the MF/HF RF band. The RF signal is low-pass filtered and amplified before being passed on to the PA/Filter Assembly (ASY-0245-02) via a coaxial cable. Transmitter preamplifier Q1 boosts the signal level sufficiently to drive the push-pull driver stage consisting of Q2 and Q3. The driver output is then routed to the push-pull power amplifiers, Q6 and Q7. The output of the amplifier is then routed through the T/R relay to a low pass filter that is relay selected for the desired band of operation. The filtered output is fed to the antenna jack on the SEA 245 rear panel.

5.3.2 THE MICROPHONE AUDIO CIRCUITRY

The 600 ohm dynamic microphone output is terminated by 620 ohm resistor R8 and then passes through R94 and C13X to the input of the amplifier/phase splitter stage

consisting of operational amplifiers U10C and U10D. MOSFET Q5 is connected between the junction of R94 and C13X and ground and serves to mute the microphone circuitry in the receive mode. The balanced audio output from U10C and U10D passes through analog gates U13A and U13D to the SEAbuss audio line. The SEABUSS audio interconnection between the Front Panel/Controller Assembly (ASY-0245-03) and the Mainboard Assembly (ASY-0245-01) is through the 8-pin ribbon cable between P2 on the Controller board and J4 on the Mainboard. These 8-pin DIP interconnections constitute an internal SEABUSS interface between the two assemblies.

5.3.3 THE AUDIO LINE RECEIVER/TRANSMITTERS

SEABUSS audio is bidirectional and passes through audio line receiver/transmitters at both ends of the path.

The receiver/transmitter circuitry consists of a balanced input line receiver and a balanced output line driver or transmitter. The line driver is connected to the SEAbuss(c) line through analog gates. These gates disconnect the line driver from the SEABUSS when the receiver/transmitter is in the receive mode. In the receive mode, balanced audio is presented to the input of an operational amplifier connected as a differential amplifier. Balanced operation permits a high degree of common mode rejection, insuring good noise rejection. The output of the line receiver is unbalanced audio which is then passed on to the internal radiotelephone circuitry.

When the receiver/transmitter circuitry is in the transmit mode, the analog gates are turned on, connecting the balanced output of the two amplifier line driver to the SEABUSS.

SEABUSS audio level is nominally 2 volts peak-to-peak balanced (0 dBm).

5.3.4 THE CODEC AND DIGITAL SIGNAL PROCESSOR

CODEC, U1, digitizes audio from the microphone circuitry at a rate of 96 kilosamples each second. The samples are transferred to the DSP U7 for processing. The DSP performs audio processing to maintain a relatively uniform audio level and to reduce the peak-to-average ratio of the audio. This facilitates more efficient use of the RF power amplifier. The audio is also bandpass filtered to remove unwanted components, particularly above 2900 Hz. The audio is then converted to a single sideband signal at the (nominal 16 kHz) subcarrier frequency. This SSB signal is then passed through the CODEC and converted to I and Q analog signals.

5.3.5 THE QUADRATURE MODULATOR

The I and Q signals from the CODEC are sent to quadrature modulator U6 on the Mainboard. This modulator consists of a PLL based LO phase shifter, two mixers and a combiner. A 45.016 MHz local oscillator (LO) signal from the synthesizer is AC coupled into the modulator. The internal PLL circuit regenerates the 45.016

MHz LO and produces two 45.016 MHz LO signals with a 90 degree phase differential. These are used as the two local oscillators for the mixers. One is mixed with the I component and the other is mixed with the Q component. The two mixer outputs are summed to complete the single sideband mixer. In the summer the desired sideband adds constructively while the undesired sideband cancels out, producing a single sideband signal with a center frequency of 45 MHz. A DC bias network with three trimpots (R77, R78, and R85) allows adjustment of opposite (image) sideband and carrier suppression.

5.3.6 45 MHz IF AND SIGNAL MIXER

The 45 MHz signal from the quadrature modulator passes through switching diode/attenuator CR6 to topping filter FIL1A/FIL1B. When in the transmit mode, CR6 is biased on by the +12VTX rail through resistors R48 and R66. Bias current is approximately 10 mA, resulting in a low loss switch. Monolithic filter FIL1A/FIL1B is matched to the low impedances of the quadrature modulator and mixer by the two "L" networks, L10/C39 and L9/C38. The filter output is passed through CR5 to a attenuator consisting of R34, R35 and R36 and then through CR4 to the IF port of MIX1

5.3.7 THE LOW PASS FILTER AND TRANSMITTER PREAMPLIER

The downconverted transmitter signal from MIX1 is passed through a seven section elliptical function low pass filter which provides some 50 dB of rejection for the image and IF frequencies above 30 MHz. The filtered MF/HF signal is then passed through diode switch CR3 to the input of the transmitter preamplifier. L6, A 27 μH choke, serves as a simple high pass filter to restrict signal into the preamplifier to the MF/HF spectrum. The transmitter preamplifier is a two-stage wide band amplifier. The first stage consists of transistors Q3 and Q4 in a negative feedback voltage amplifier. The output of this stage is taken from the low impedance emitter of Q4 and further amplified by Q5. Q5 is a transformer coupled power amplifier which is used to boost the power output level of the SSB signal to the approximately 4 mW (+6 dBm) required by the PA/Filter Assembly (ASY-0245-02). The signal exits the Main Board via coaxial cable and enters the PA/Filter board on J1.

5.3.8 THE TRANSMITTER PREDRIVER

The low level transmitter signal is routed from J1 through a 3 dB pad and a wideband transformer (T1) to the base of Q1. Q1 is a 2N3866 connected in the common emitter configuration and is transformer coupled to the push-pull driver stage. Bias for Q1 is provided by the base resistor network with R6 used to adjust the idling (no signal) current in the device to 60 mA (0.275 volts across R7/R8). The emitter resistor (R7/R8) is used together with press-on heat sink to provide thermal stability for Q1.

5.3.9 THE TRANSMITTER DRIVER

Transistors Q2 and Q3 are small plastic RF power devices connected as a push-pull common emitter amplifier. Transformer T2 provides push-pull base drive from the predriver, while transformers T3 and T4 provide DC power isolation and collector to load impedance matching, respectively. Gain/bandwidth compensation is provided by the collector/base feedback networks and the various peaking capacitors and terminating resistors. Temperature tracking bias is provided for Q2 and Q3 by the circuitry associated with Q4 and Q5. Q4 is a small silicon power transistor connected as a voltage amplifier and buffered by power emitter follower Q5. The current in Q4 is proportional to temperature. This causes the collector voltage to drop as heat sink temperature rises. The collector voltage is the source of base drive for the bias buffer emitter follower Q5. Bias current for Q2 and Q3 is adjusted to 140 mA by the potentiometer, R14, in the emitter circuit of Q4. Collector voltage for Q4 is derived from the +10VTX bus, while collector voltage for Q5 is derived from the +12VTX rail.

5.3.10 THE TRANSMITTER POWER AMPLIFIER

The power amplifier in the SEA 245 is a push-pull common emitter design with a temperature stabilized bias source. The amplifier runs from the +24 volt input and has the collector voltage present at all times. The amplifier is activated by turning on the various bias supplies when in the transmit mode.

Since the +24 volt power source is isolated from the chassis, the power amplifier bias generator must be powered from the +24 volt rail. The bias generator circuitry consists of Q8, Q9 and regulator U4. +24 volt power for U4 and Q8 is switched by the +12VTX rail through Q12 by optical isolator U5. When the +12VTX rail is high U5 turns on Q12, energizing the bias generator circuitry. Q8 serves as a power emitter follower to buffer the voltage generated by the temperature-tracking amplifier, Q9. Q9 is a small power transistor that is thermally linked to the power amplifier heat sink. To insure stability in the presence of varying line voltages, the collector voltage for Q9 is obtained from 9 volt regulator U4. R28 permits adjustment of the idling (no signal) current in Q6 and Q7 to 150 mA.

5.3.11 THE OUTPUT LOW PASS FILTERS

Five low pass filters are provided to cover the frequency range from 1.6 - 30 MHz. Note that the highest frequency filter, which covers the-26 - 30 MHz spectrum, is a 3-pole elliptical function design, while the lower frequency filters are 7 pole elliptical function types. This is possible because of the natural drop in spurious outputs from the power amplifier at higher frequencies. Filter selection is through small power relays, which are operated by the Mainboard controller computer through a serially loaded relay driver consisting of shift register U2 and buffer-driver U3.

5.3.12 THE ALC CIRCUITRY

The transmitter ALC circuitry is DSP based. The control signals for the ALC system are derived from the dual directional coupler consisting of transformers T13 and T14 and termination resistors R44, R47 and R48. The forward power signal is detected by CR3 and scaled by resistors R49 and R50 before being buffered by U1B. The reflected power signal is detected by CR4 and buffered by U1A. The buffered analog voltages corresponding to forward and reflected power levels are then routed through the Mainboard to A/D converter inputs on the CPU board microprocessor, U5.

5.4 THE MASTER CLOCK OSCILLATOR AND SYNTHESIZER SYSTEM

5.4.1 BLOCK DIAGRAM

Figure 5.4.1 shows the block diagram of the local oscillator system of the SEA 245.

The block diagram illustrates a total of two synthesizers. The first local oscillator operates from 45 to 75 MHz and uses three bandswitched VCOs. These are controlled by synthesizer chip, U21, which contains a dual modulus divide-by-N counter, a variable modulus reference counter and a phase detector. The basic reference rate for the phase detector is 8 kHz, which sets the "coarse" step size for the first local oscillator to 4 kHz. (The VCO signal tunes from 90 to 150 MHz and is divided by two before being applied to the first mixer.)

The second local oscillator synthesizer operates at 45.040 MHz with a reference rate of 8 kHz.

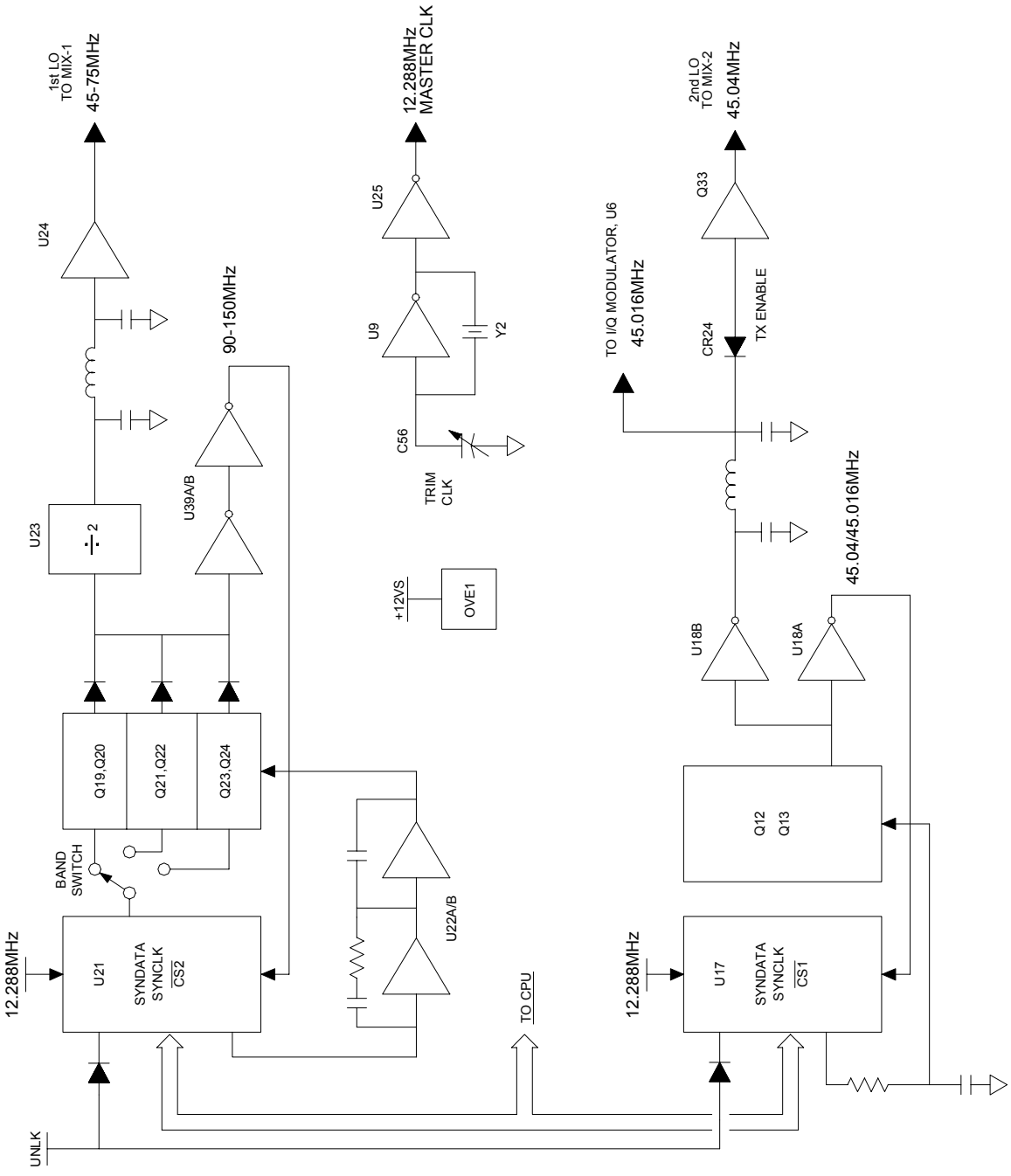
5.4.2 THE MASTER CLOCK OSCILLATOR

Primary frequency control is maintained through a master temperature-stable crystal oscillator (TCXO) operating at 12.288 MHz. Clock stability is achieved through a combination of temperature control and temperature compensation. The Master Clock Oscillator crystal Y2 is mounted in a proportional oven to insure stability. Unbuffered HCMOS U9 and U25 gates are used for both oscillator and buffer amplifier functions. Trimmer capacitor C56 is used to set the clock frequency.

5.4.3 THE FIRST LOCAL OSCILLATOR SYNTHESIZER

The first LO synthesizer consists of three switched VCOs, a buffer amplifier and a phase locked loop circuit. The synthesizer generates local oscillator frequencies from 45.4 - 75.0 MHz corresponding to operating frequencies of 0.4 - 30.0 MHz. The oscillators themselves operate at twice the desired output frequency, however. Operation of a typical VCO is described below. Q23 is configured as a Colpitts oscillator with inductor L35 and varactor diode CR15 serving as the frequency determining elements. Q24 buffers the VCO to prevent load pulling. These components make up the highest frequency VCO, which tunes from approximately 130 to 150 MHz.

Switch transistors Q16, Q17 and Q18 provide power to the selected VCO. The base of Q18 is pulled low through R146 supplying 10 volts to the HIGHBAND VCO, Q23-Q24. When the MIDBAND VCO is selected, Q13 will be turned on by a high on pin 16 of U21. This will pull the base of Q17 low, energizing Q21 and Q22. At the same time the base of Q18 is pulled high through diode CR10 switching OFF the HIGHBAND VCO. Similarly, selection of the LOWBAND VCO is accomplished by a high on pin 15 of U21, which turns on Q14/Q16, supplying power to Q19/Q20 and



SEA 245
Synthesizer Block Diagram
Figure 5.4.1

holding OFF the HIGHBAND VCO through diode CR10. Steering diodes CR17 and CR18 are used to provide isolation between the two OFF VCOs and the active output.

The output from the selected VCO is passed through prescaler, U23 where the signal is divided by two. The prescaler output is buffered by MMIC, U24, before being sent to the first mixer. The VCO output is also passed through dual buffer amplifiers U39A and U39B. The output signal from U39B provides the VCO signal to the synthesizer chip U21. Using separate amplifiers in this fashion improves the isolation between the receiver mixer circuitry and the input to the synthesizer chip.

Serially loaded PLL chip U21 provides a reference counter, divide-by-N counter, a phase/frequency detector and the VCO control register. The PLL reference frequency is derived from the 12.288 MHz Master Clock. Loop filtering and level shifting of the PLL phase detector output is accomplished by active filters U22A/B.

5.4.4 THE SECOND LOCAL OSCILLATOR SYNTHESIZER

The second local oscillator synthesizer consists of PLL chip U17, 45.040 MHz Colpitts oscillator FET Q12, and buffer amplifier Q13, U18A, U18B and Q33. Buffer amplifier U18A provides a sample of the 45.040 MHz VCO signal for the synthesizer chip while U18B provides 45.040 MHz drive for the second mixer.

5.5 THE 2187.5 kHz MONITOR RECEIVER

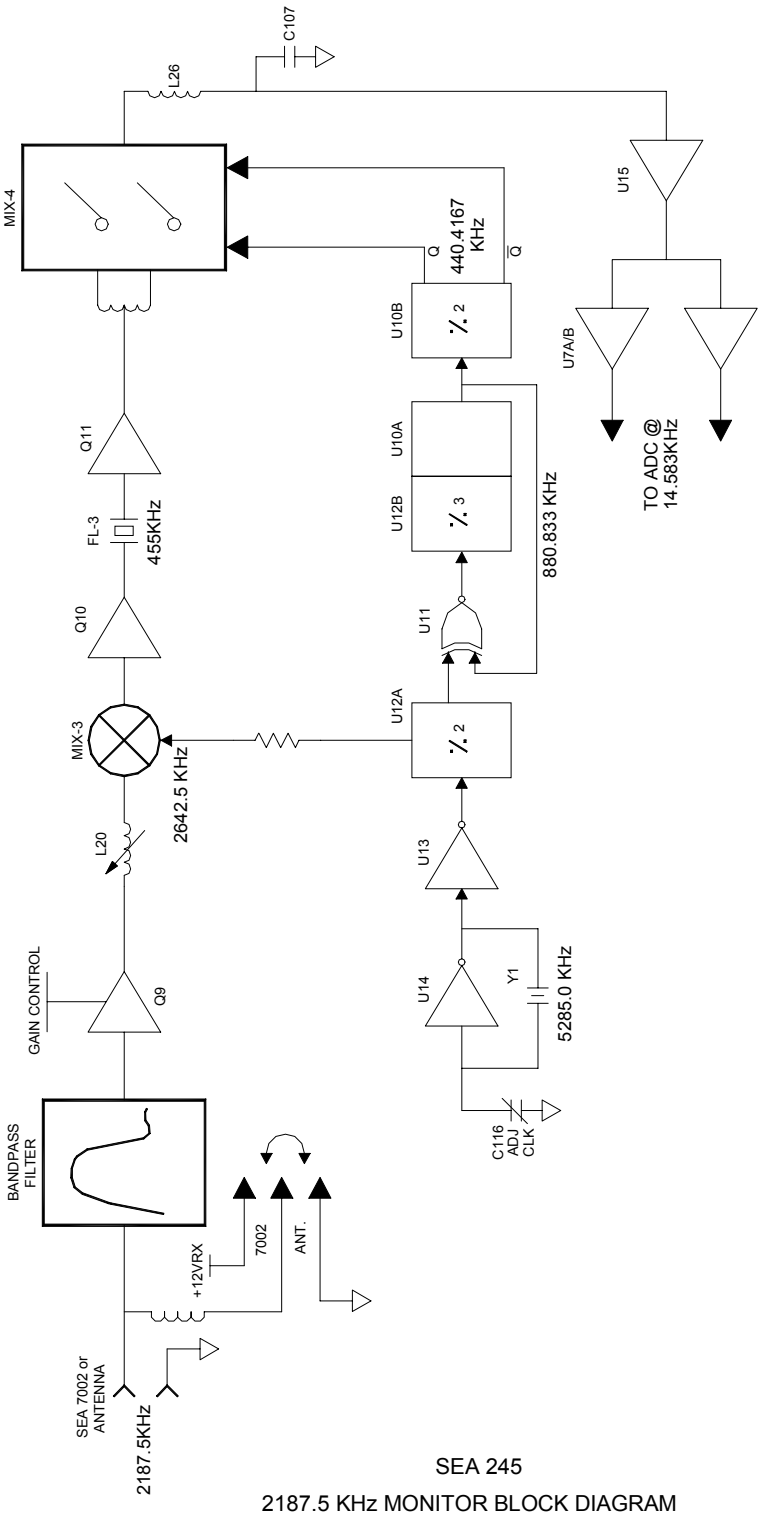
5.5.1 BLOCK DIAGRAM

Figure 5.5.1 shows the block diagram of the 2187.5 kHz monitor receiver, required for GMDSS applications is Sea Area 2. The receiver is a single channel, dual conversion design which uses a single crystal to provide both conversion signals. The first IF frequency is 455 kHz, the second IF frequency is nominally 14.583 kHz. As in the SEA 245 Main Receiver, the DSP engine provides all channel selectivity, signal demodulation, and AGC.

5.5.2 RECEIVER RF CIRCUITRY AND FIRST MIXER

Antenna input to the 2187.5 monitor receiver is on pins 13 (signal) and 14 (ground) of the rear panel Accessory Connector. The impedance is 50 ohms and provisions have been made to support the SEA 7002 Active Antenna, should this be desired.

The RF signal first passes through a high pass filter and then a low pass filter to Q9, the preamplifier. The preamplifier is a grounded-gate JFET with tuned drain circuit. The nominal gain of this stage is about 8 dB with the drain voltage on. As in the Main Receiver, a gain step is provided by switching the drain voltage off under control of the AGC program in the DSP. The combination of the front end 5-section low pass filter and the low pass response of the preamplifier drain circuitry combine to provide the receiver with better than 75 dB rejection of the 3097.5 kHz primary image.



SEA 245

2187.5 KHz MONITOR BLOCK DIAGRAM

Figure 5.5.1

The first mixer is a conventional +7 dBm double balanced type, which provides excellent dynamic range in this application.

5.5.3 THE 455 kHz IF AMPLIFIER

The first 455 kHz IF amplifier is Q10, a grounded-gate JFET which provides some gain and serves as a wideband 50 ohm termination for the mixer. The output from the amplifier is passed through FL3, a 6-pole ceramic bandpass filter with a nominal bandwidth of 4 kHz. Output from the filter is then passed through emitter follower Q11 to the second mixer.

5.5.4 THE SECOND MIXER/POST AMPLIFIER

The second mixer is a double balanced commutation mixer, which uses a quad HCMOS analog gate (U16) as the switching element. Push-pull signal drive is provided to the two switch arms through a wideband transformer. (Note that two gate elements are used in each switch arm.) Push-pull local oscillator drive is applied to the switch actuator pins from the output of the local oscillator divider chain. Both output arms of the switch are summed together, resulting in a double-balanced switching mixer with excellent dynamic range and good local oscillator balance.

Output from the mixer is passed through a low pass filter consisting of L26 and C107 to a low noise operational amplifier stage with gain of 10 and a phase splitter, which, as in the Main Receiver, drives the A/D input.

5.5.5 THE LOCAL OSCILLATOR CIRCUITRY

Both conversion oscillator frequencies are derived from the same crystal controlled source in the following fashion. Crystal oscillator U14 operates at 5285.0 kHz. This oscillator is temperature compensated and maintains a frequency stability of less than ±4 ppm over the voltage and temperature range of the equipment. Trimmer capacitor C116 is used to set the oscillator frequency to exactly 5285.0 kHz at TP10. Output from the oscillator is buffered by gate U13 and then divided to 2642.5 kHz by U12A. This signal is sent to both the first mixer and the second local oscillator divider chain. The difference frequency between the first local oscillator and the 2187.5 kHz signal frequency is 455 kHz.

U11, U12B and U10A form a symmetrical divide-by-three counter. The resulting 880.3333 kHz signal is then further divided by two in U10B. The Q and notQ outputs of U10B are at 440.4167 kHz and, when mixed in MIX-4 with the 455 kHz IF signal, results in the 14.5833 kHz last IF frequency which is amplified by U3 and U5A/B and then sent through the A/D converter to the DSP for further filtering and demodulation.

5.6 THE POWER SUPPLY CIRCUIT

5.6.1 GENERAL

The basic supply voltage for the SEA 245 is a floating ground 24 Volt DC source. Line voltage regulation of ±15% or better is required, with a current capacity of at least 15-20 amperes. From this raw source are derived the necessary regulated operating voltages for the SEA 245 circuitry.

5.6.2 BLOCK DIAGRAM

Figure 5.6.1 shows a simplified schematic diagram of the power supply circuitry.

Once the basic 24 Volt DC power is provided, it is connected to the set through the heavy-duty power plug on the transceiver rear panel. A variety of internally mounted fuses are provided to protect the set in the event of malfunction. The primary line fuses are equipped with a polarity protection diode that will blow the line fuses in the event of reversed line polarity.

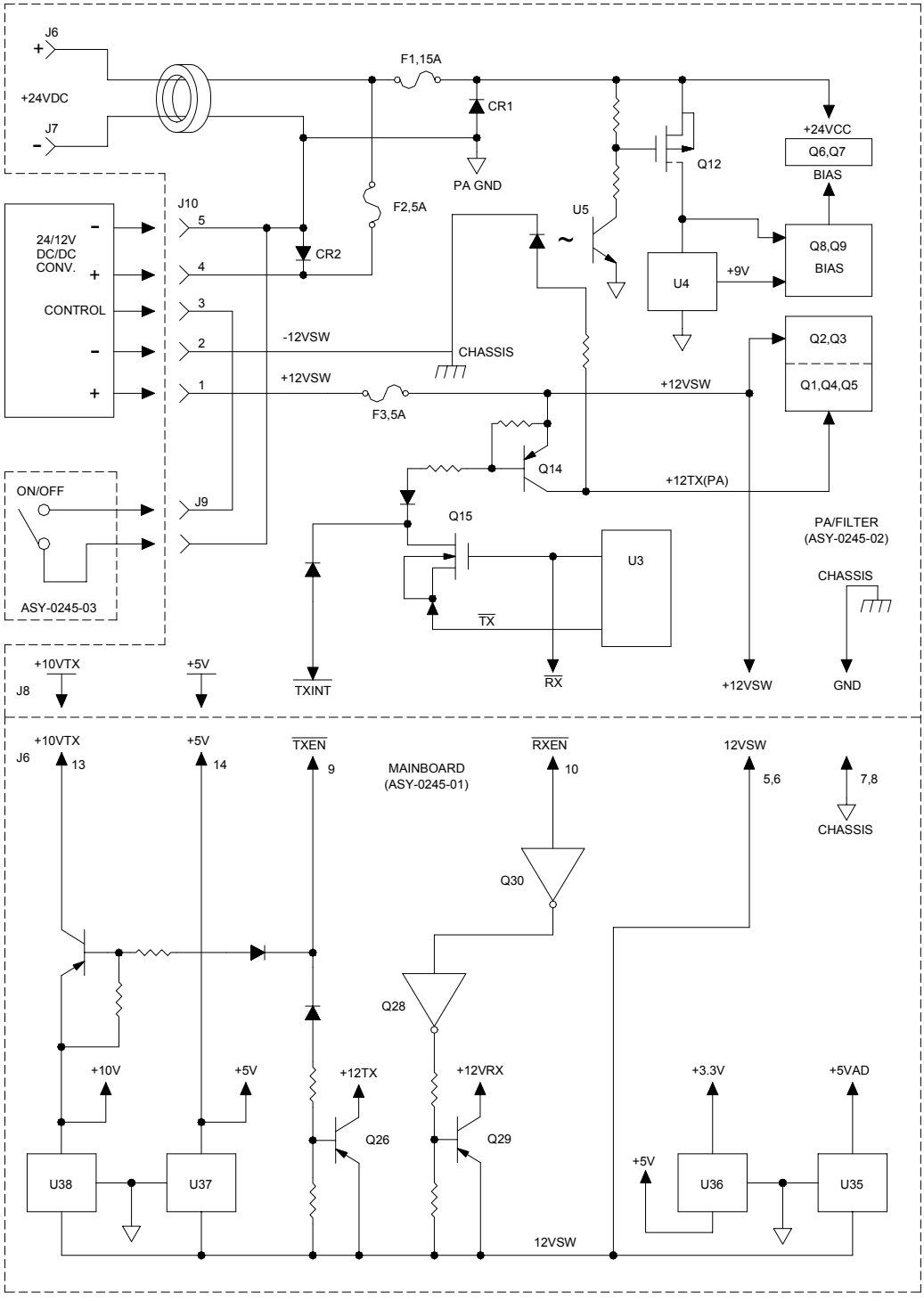
As illustrated in Figure 5.6.1, the 24 Volt DC power from the rear panel mounted connector passes through a ferrite line filter to the PA/Filter Board (ASY-0245-02) where the power is distributed to the internal circuitry through fuses F1 and F2.

15 ampere fuse F1 serves to protect the circuitry associated with the output stage of the power amplifier. 5 ampere fuse F2 protects the primary circuitry for the isolated 24/12 volt DC/DC converter which provides the regulated, chassis referenced, +12 volt rail. The +12 volt rail powers the low level circuitry in the SEA 245. Each fuse is individually protected from reverse polarity by power diodes CR1 and CR2 and each power rail is individually filtered by 470 μF capacitors C29 and C47. Note that these rails are NOT switched. Power is present on the power amplifier module and the DC/DC converter input AT ALL TIMES.

5 ampere fuse F3 protects the regulated +12 volt primary power distribution system in the SEA 245. Capacitors C75, C76 and C78 serve as line filters. The fused, filtered +12 volt regulated rail is designated the +12VSW line and is distributed to the SEA 245 circuitry through pins 5 and 6 of J8 on the PA/Filter Assembly. (Ground and negative rail use pins 7 and 8).

5.6.3 THE MAIN POWER CONTROL CIRCUITRY

The main power switch in the SEA 245 is the ON/OFF switch located on the front panel VOLUME control. Wires from the switch connect to J9 on the PA board (ASY-0245-02). When the front panel switch is closed by rotating the VOLUME control to the right from the stop, a connection is made between J10 pins 1 and 3. This turns the 24/12 volt DC/DC converter ON and powers up the +12VSW rail in the SEA 245.



SEA 245
Power Distribution Block Diagram
Figure 5.6.1

5.6.4 +10 VOLT REGULATOR AND THE +10VTX SWITCH

The internal +10V rails are derived from the +12VSW buss through regulator U38. The +10VTX rail is generated by inverted switch Q27. Grounding the notTXEN line will turn on Q27, enabling the +10VTX rail. The notTXEN line comes from the PA/Filter Assembly through pin 9 of J6.

5.6.5 +12 VOLT RAIL AND THE +12VTX/+12VRX SWITCHES

Transistors Q26 on the mainboard generate the mainboard +12VTX rail. The +12VTX rail is energized when the notTXEN line from pin 9 of J6 goes low, switching Q26 on.

The +12VRX rail is energized when the notRXEN line from pin 10 of J6 goes low. This turns Q30 off which turns Q28 on, switching Q29 on.

The use of transistor switches to generate the TX and RX rails eliminates any problems with relay contacts or T/R timing.

5.6.6 +5 VOLT REGULATORS

The +5 volt rail for the Mainboard Assembly and the PA/Filter Assembly is derived from the +12VSW rail through regulator U37.

In the Front Panel/Controller Assembly (ASY-0245-03) a separate 5 volt regulator, U16, provides the regulated rail for the controller circuitry. Note that the controller +12VSW rail comes through the standard SEABUSS interconnection.

5.6.7 +3.3 VOLT REGULATOR

U36 on the Mainboard Assembly provides the +3.3V rail which is used in the CPU/DSP Board (ASY-0245-04) to power the main control computer hardware.

5.6.8 +12VTX RAIL

The transmitter predriver circuitry and the bias systems for the transmitter driver are supplied with a relatively high current +12VTX rail through Q14. Q14 is a PNP power transistor, operated as an inverted switch. Base drive for Q14 is provided by the INTERLOCKED notTX line. This line is obtained through the "safety clamp' transistor, Q15, from the notTX and notRX ports generated by the controller computer through the shift register U2 and the buffer chip, U3. When the notTX port from pin 16 of U3 is LOW and the notRX port from pin 5 of U2 is HIGH, the INTERLOCKED notTX line is LOW. This will cause Q14 to be ON, energizing the +12VTX rail.

Note that the INTERLOCKED notTX line is also used to control Q26 and Q27, the +12VTX and +10VTX switch transistors respectively, on the Mainboard Assembly. The use of the INTERLOCKED NOT TX line in this fashion prevents the simultaneous application of +12VTX and +12VRX to the low level transceiver

circuitry.

5.6.9 THE +24VTX RAIL AND PA BIAS SYSTEM

Bias for the PA output transistors is generated from the +24VTX rail. Since the entire +24 volt power source is isolated from the chassis, an optical isolator, U5 on the PA/Filter Assembly (ASY-0245-02) is used to switch on a P-channel FET (Q12) when the +12VTX rail is energized. This +24VTX line is then used to power bias regulator transistor Q8 and the +9V PA bias supply regulator U4. The output from U4 powers bias tracking amplifier transistor Q9. Q9 is a small power device which is bonded to the same heat sink as the RF power transistors to provide thermal feedback.

5.7 THE MAINBOARD CONTROLLER AND DSP PROCESSORS

5.7.1 GENERAL

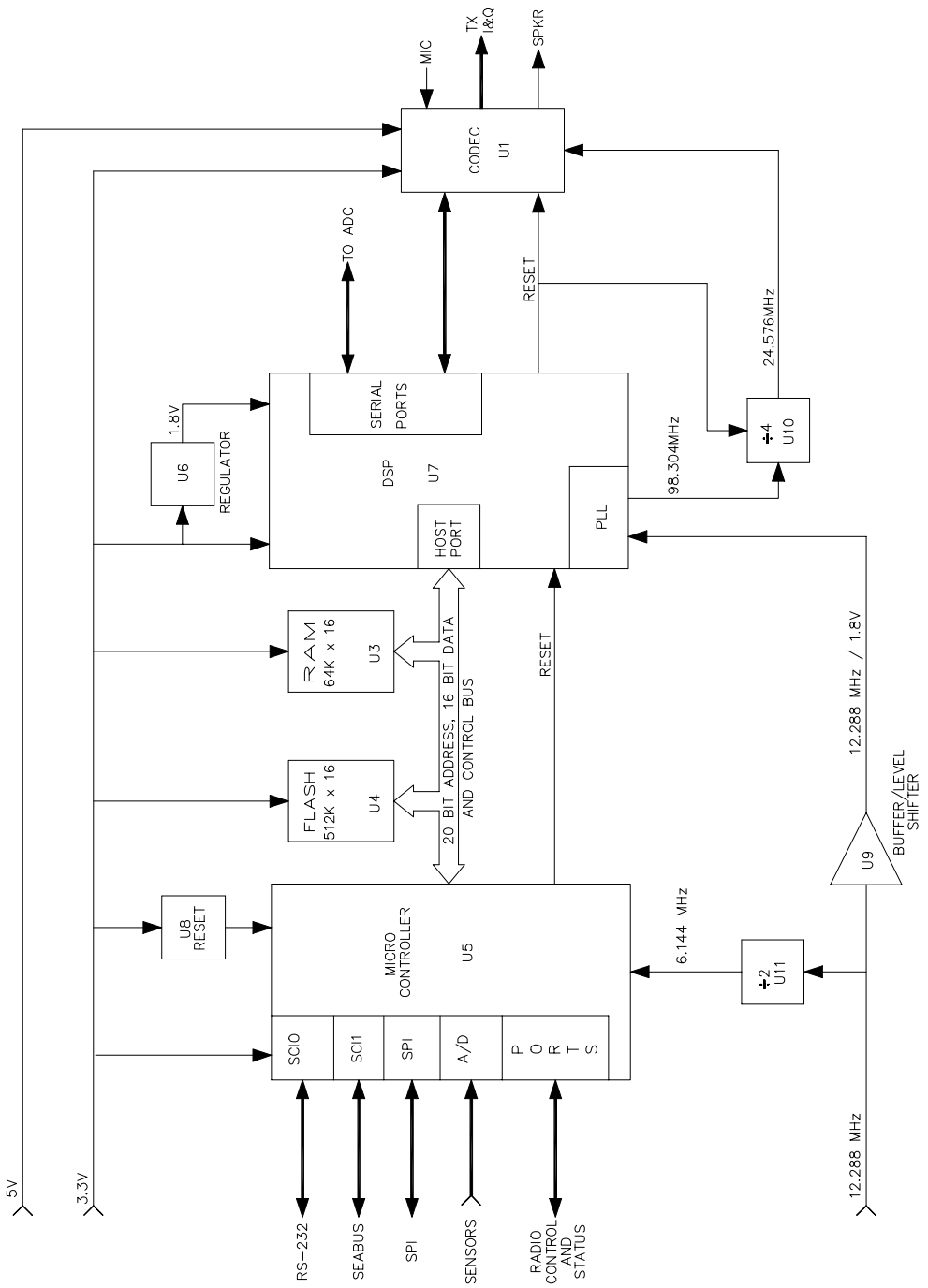
The Mainboard microcontroller and digital signal processor (DSP) are contained on a separate assembly (ASY-0245-04). The microcontroller is a Motorola MC68C812A4 operating from a 6.144 MHz clock. This is a low voltage (3.3V) 16-bit processor with two asynchronous serial ports, a serial peripheral interface (SPI), a timer and pulse accumulator module, an 8-channel 8-bit A/D converter, 1 Kbyte of RAM, 4 Kbytes of EEPROM and memory expansion logic with chip selects. It also has many bidirectional ports for general purpose I/O. The DSP is a TI TMS32OVC5402. This is a 32-bit fixed-point DSP capable of 100 MIPS operation. It includes 16 Kwords (16-bit) of internal RAM, two sophisticated multichannel serial ports and a parallel host port interface.

5.7.2 BLOCK DIAGRAM

Figure 5.7.1 shows a block diagram of the processor assembly.

5.7.3 CLOCK DISTRIBUTION

The 12.288 MHz master clock is supplied through P2 to the processor assembly (ASY-0245-04). U11A divides this clock by two to provide a 6.144 MHz clock to the microcontroller, U5. U9 buffers the clock and converts it to a 1.8 volt level suitable for the DSP, U7. The DSP has an internal PLL which generates a 98.304 MHz clock phase locked to the 12.288 MHz reference. The 98.304 MHz clock is used as the cycle clock for the DSP and is also divided by 4 by U10 to produce a 24.576 MHz clock for the CODEC, U1. This clock divider can be reset by the DSP in order to insure a known phase relationship between the CODEC clock and the DSP clock. This is necessary for reliable communication between the CODEC and the DSP.



SEA 245 Processor Assembly
Block Diagram
Figure 5.7.1

5.7.4 MICROCONTROLLER OPERATION

Reset generator, U8 provides a reset pulse to microcontroller U5 at startup or if there is a dip in the power supply. At startup the microcontroller has access only to the internal resources. It runs software contained in the internal EEPROM. This software configures the chip and either boots a program from the RS-232 port (Useful for service and reprogramming functions) or transfers control to the flash memory. The flash memory contains most of the software for running the radio. The radio channel list also resides in flash as well as software to be downloaded to the DSP. A 64 kword external RAM is provided for workspace and stack space. Additional memory for scratchpad channel storage and radio configuration parameters is contained in the nonvolatile internal EEPROM. The microcontroller may also communicate with the DSP as a memory-mapped device on the bus.

The processor has two asynchronous serial interfaces (SCI's). SCI0 is used to provide an RS-232 interface to the radio which can be used for computer control or for reprogramming the flash memory. SCI1 is used to provide a SEABUSS interface to the front panel or a remote controller. The processor also has a serial peripheral interface (SPI) which is used to communicate with the synthesizers as well as a shift register which provides control signals to the PA/Filter Assembly.

The processor has an 8-channel analog to digital converter port. Not all of these A/D converter channels are in use but some of them are used to read temperature sensors, power sensors and synthesizer lock detection signal ports.

Finally there are quite a few general purpose I/O ports used to control the radio. For example these are used to control gates to route audio signals, to communicate with an Automatic Antenna Tuner, to control receiver gain steps, to switch the cooling fan and the reset the DSP.

5.7.5 DSP OPERATION

At startup the DSP, U7, is reset by a port signal from the microcontroller, U5. The microcontroller then transfers the firmware from the flash memory, U4, to the DSP via the host port interface on the microcontroller's bus. This firmware runs out of the DSP's internal RAM.

The DSP has two serial ports. One of these is used to communicate with the previously described A/D converter on the Mainboard. This stereo 24-bit converter samples signals from the Main Receiver and the Watch Receiver 96000 times per second. During each sample two 24-bit words (One for each receiver) are transferred over the serial port to the DSP. The DSP generates the 96KHz clock which provides a framing signal to the A/D to select between the two channels. The other serial port is connected to the CODEC, U1, which is described further below. The interface is similar to the A/D interface but the sample rate is 48 KHz.

The operation of the DSP depends on whether the radio is receiving or transmitting. When receiving the DSP reads receiver samples from the A/D. The digitized SSB

samples are processed to convert them to the audio band, filter out undesired signals and provide gain control and noise blanking. Watch Receiver signals are also FSK demodulated in order to detect Digital Selective Calling (DSC) data. Audio samples from the Main Receiver are passed to the speaker audio circuit through the CODEC monophonic output. DSC data is passed to the microcontroller over the host port for further data decoding. In transmit mode microphone audio samples are read by the DSP from the CODEC, U1. the DSP performs speech processing on these samples and converts them to inphase and quadrature signals at an IF of approximately 15 KHz. These I and Q samples are transferred to the I/Q Modulator through the CODEC.

In both transmit and receive modes, the DSP also communicates regularly with the microcontroller over the host port. In receive mode the DSP regularly sends gain information to the microcontroller as well as DSC data. In the transmit mode the DSP must obtain power sensor data from the microcontroller in order to implement Automatic power Level Control (ALC). The DSP also receives mode information from the microcontroller which determines operating parameters of the DSC such as PTT status, transmitter power level and receiver bandwidth.

5.7.6 CODEC OPERATION

U1 is an AC '97 compliant 18-bit stereo CODEC operating with a 48 KHz sample rate. On board multiplexers can select between two stereo inputs and three mono inputs. It also has selectable stereo or mono outputs. Each channel has independent gain and mute controls. All of the control and status as well as the stereo input and output sample data is passed over the serial connection to the DSP. the stereo output is used for transmit I and Q samples for the modulator. The mono output is used for speaker audio. Two of the inputs are used for microphone audio and an alternate low level audio input. The other input channels are not used.

6 THE SEA 245 FRONT PANEL/CONTROLLER SYSTEM

6.1 GENERAL

The SEA 245 Front Panel/Controller unit is a complete SEABUSS controller and is designed in such a manner as to permit direct installation on the front of a standard SEA 245 as well as in remote installations. The SEA 245 will support a SINGLE remote controller and a SEABUSS compatible Antenna Tuner such as the SEA 1631. The maximum TOTAL length of SEABUSS cable not to exceed 200 feet (60 meters). The stand-alone Controller (SEA 2450) is designed for shipboard mounting. Keypad and display are backlighted for operator convenience

Figure 6.1 shows the outline dimensions of the SEA 2450 with mounting bracket. For information regarding flush mounting, contact the SEA, Inc. factory.

Interconnection between the Front Panel/Controller and the SEA 245 Mainboard Assembly (ASY-0245-01) when the Controller is directly attached to the radiotelephone is through an 8-pin DIP connector which carries the standard SEABUSS interface connections (See Front Panel/Controller (ASY-0245-03) schematic diagram). This connector (P1) connects to connector J3 on the Mainboard Assembly (ASY-0235-01) through a short, 8 conductor ribbon cable.

Remotely located Controllers use the standard 9-pin Phoenix style SEABUSS connector and interconnection is, as stated above, through standard SEABUSS cable (CAB-2350-XX). The recommended cable is designed to provide adequate interconnection for the +12VSW line and the PTT line, as well as providing two shielded, twisted pairs to support the SEABUSS audio circuit and the SEABUSS data circuit. Note that all SEABUSS cable interconnections are pin-for-pin and that the shielded twisted pairs are used for audio and data interconnection. See Figures 4.5 and 4.6 for details regarding system interconnections.

6.2 THEORY OF OPERATION

Figure 6.2 shows a block diagram of the Front Panel/Controller Assembly.

The controller(s) are essentially "dumb terminals" configured specifically as the front panel of a Single Sideband Transceiver. Radiotelephone functions are controlled by the keypad, transceiver parameters are indicated by the liquid crystal display (LCD), microphone audio is processed by the circuitry on the Front Panel/Controller PC board and then routed to the transceiver circuitry through the SEABUSS audio interconnection, and receiver audio is received from the transceiver through the SEABUSS audio interconnection and then processed through the volume control, squelch gate and loudspeaker amplifier to the loudspeaker.

The controller circuitry is contained on the Front Panel/Controller PC assembly (ASY-0245-03). This printed circuit board contains the keyboard interface,

microphone audio to SEABUSS and SEABUSS to loudspeaker audio circuitry, the LCD display and display driver circuitry and the controller CPU.

The primary power source for the Front Panel/Controller Assembly is the +12VSW buss from the SEA 245 Mainboard Assembly. This power buss is part of the SEABUSS interconnection.

Most of the Front Panel/Controller circuitry operates from a +5 volt regulated line derived from the +12VSW rail through regulator, U16. The SEABUSS PTT line is a buffered output from the Front Panel/Controller board CPU. When the controller microphone requests PTT, the controller CPU processes this request and signals the SEA 245 Mainboard Assembly through buffer amplifier Q7.

6.2.1 KEYBOARD SUPPORT

The SEA 245/SEA 2450 keyboard has a total of 19 keys. Key status is determined by scanning the matrix through control lines from the CPU chip, U1.

6.2.2 THE LCD DISPLAY AND DISPLAY LIGHTING

DISPLAY: The front panel display is a LED backlighted LCD graphic module. Various display configurations are provided which permit the operator to monitor all the various radiotelephone parameters such as channel number, power level, memory mode, etc. The display is controlled by the Front Panel/Controller microprocessor, U1. Display contrast is controlled through U1 by a voltage level from D/A converter chip U6 and operational amplifier U17A. This trimming voltage is applied to Vo (Pin 3 on connector P7).

BACKLIGHTING: Similarly, the backlighting level is controlled through microprocessor U1 by a voltage level from D/A converter chip U6 and emitter follower Q2. This control voltage is applied to the base of control transistors Q3 and Q4. Varying the control voltage will vary the current through the backlighting LEDs, thus adjusting the backlight level.

6.2.3 THE SQUELCH FUNCTION

In the SEA 245/SEA 2450, the squelch function is a software voice-operated "constant SINAD" squelch system which functions by examining the audio stream to determine the presence of a voice signal.

A sample of the receiver audio from the SEABUSS audio receiver (U10A) is amplified and limited by U9A/B, processed by the software routine running in U1 and used to control the audio to the volume control. When the squelch program senses that a signal is present, the control signal to the gate of shunt transistor Q6 goes LOW, permitting audio to pass. Although the computer controlled squelch is relatively immune to changing noise conditions, in some cases it may be advantageous to reset the squelch trigger threshold. This is a software function and may be accomplished through the keypad. (See operator's instructions).

6.2.4 BILATERAL AUDIO CIRCUITRY

The receiver audio path in the Front Panel/Controller Assembly is from the bilateral, balanced SEABUSS audio terminals (P1, Pins 6 and 7), through the balanced to unbalanced audio line receiver (U10A), the squelch gate (Q6), the volume control (R2) and the audio power amplifier (U14) to the loudspeaker. The squelch limiter (U9A and U9B) connects to the audio upstream of the squelch gate. The hard limited output of the limiter is connected to the input of the controller CPU, U1.

The transmitter audio path is from the microphone to the microphone mute transistor (Q5) and from there on to the microphone amplifier/SEABUSS driver consisting of U10C and U10D. SEABUSS audio level is nominally 2.0 volts peak-to-peak (0dBm).

6.2.5 SEABUSS DATA CIRCUITRY

The serial data stream which links the controller(s) and the transceiver connects to the controller(s) at P1, Pins 4 and 5. The data transducer is a bidirectional data transceiver (U6) which uses a bi-phase data format similar to RS485. On each end of the data path, the data transceivers are connected to the system CPU boards through the Sout and Sin pins on the data transceiver. Communications between the controller(s) and the SEA 245 Mainboard Assembly are bidirectional and fully interactive. This means that when the SEA 2450 Remote Controller is used, the status of the SEA 245 is reflected at both operating stations. Controller-SEA 245 data is sent in packets and is error checked. Collision protection is provided for all data sources. Baud rate is 9600 bps. For further data on the format of the SEABUSS command structure used in the SEA 245, contact SEA, INC. at 7030 220th St. S.W., Mountlake Terrace, WA, 98043. Or call (425) 771-2182.